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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,294	04/27/2004	Terry L. Frederick	BUR920040012US1	3293

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EXAMINER	
LEVIN, NAUM B	
ART UNIT	PAPER NUMBER
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/709,294	FREDERICK ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/709,294 and Amendment filed on 02/07/2007. Independent claims 1, 8, 15 have been amended and include additional limitation. Claims 1-20 remain pending in the application.

2. The Examiner finds Applicant's arguments on the applications of Allen as none persuasive. Allen's reference reads on the claims 1-20 as presently written.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being unpatentable by Allen et al. (US Publication No.: 20050050500).

4. As to claims 1, 8 and 15 Allen discloses:

(1) A method for correcting a ground rule violation for a target via pair in design, the method comprising steps of:

identifying a target via pair the violates a ground rule (The invention can also be used to eliminate certain undesirable structures such as stacked vias or can be used to fix other problems such as insufficient via-to -via spacing – Abstract; The invention first locates stacked vias by determining which vias are positioned above or below vias in

adjacent wiring levels of the integrated circuit design (using a shapes-processing program) – [0007]; the invention first uses a shapes-processing program to find vias of interest … sets of vias that should be further spaced apart – [0025]); (Abstract; [0007]; [0025]); then

generating a redundant via for a target via (the invention forms redundant via 20 to the left of via 10. This creates space for redundant via 21 which is a redundant via of via 12 – Fig.2, [0029]; the invention adds a redundant via … this process is similar to the process of adding redundant vias discussed above – Fig.8, [0037]) of the target via pair (The invention first locates stacked vias by determining which vias are positioned above or below vias in adjacent wiring levels of the integrated circuit design – [0007]; the invention first uses a shapes-processing program to find vias of interest … sets of vias that should be further spaced apart – [0025]) where the redundant via corrects the ground rule violation (The invention can also be used to eliminate certain undesirable structures such as stacked vias or can be used to fix other problems such as insufficient via-to -via spacing – Abstract; the invention adds a redundant via and then removes the original via. In this way, vias on level Vx and Vx+1 will then no longer overlay each other - Fig.8, [0037]) (col.1, ll.49-54; col.4, ll.40-44; col.4, ll.55-57; col.5, ll.57-67; col.6, ll.1-7); (Abstract; [0002]; [0007]; [0025]; [0028]; [0029]; [0037]; [0038]); and

removing the target via corresponding to the redundant via to correct the ground rule violation (the invention adds a redundant via and then removes the original via. In this way, vias on level Vx and Vx+1 will then no longer overlay each other - Fig.8, [0037]) ([0007]; [0037]);

(8) A system for correcting a ground rule violation for a target via pair in design, the system comprising steps of ([0039]):

means for identifying a target via pair the violates a ground rule (The invention can also be used to eliminate certain undesirable structures such as stacked vias or can be used to fix other problems such as insufficient via-to -via spacing – Abstract; The invention first locates stacked vias by determining which vias are positioned above or below vias in adjacent wiring levels of the integrated circuit design (using a shapes-processing program) – [0007]; the invention first uses a shapes-processing program to find vias of interest … sets of vias that should be further spaced apart – [0025]); (Abstract; [0007]; [0025]);

means for generating a redundant via for a target via (the invention forms redundant via 20 to the left of via 10. This creates space for redundant via 21 which is a redundant via of via 12 – Fig.2, [0029]; the invention adds a redundant via … this process is similar to the process of adding redundant vias discussed above – Fig.8, [0037]) of the target via pair (The invention first locates stacked vias by determining which vias are positioned above or below vias in adjacent wiring levels of the integrated circuit design – [0007]; the invention first uses a shapes-processing program to find vias of interest … sets of vias that should be further spaced apart – [0025]) where the redundant via corrects the ground rule violation (The invention can also be used to eliminate certain undesirable structures such as stacked vias or can be used to fix other problems such as insufficient via-to -via spacing – Abstract; the invention adds a redundant via and then removes the original via. In this way, vias on level Vx and Vx+1

will then no longer overlay each other - Fig.8, [0037]) (col.1, ll.49-54; col.4, ll.40-44; col.4, ll.55-57; col.5, ll.57-67; col.6, ll.1-7); (Abstract; [0002]; [0007]; [0025]; [0028]; [0029]; [0037]; [0038]); and

means for removing the target via corresponding to the redundant via to correct the ground rule violation (the invention adds a redundant via and then removes the original via. In this way, vias on level Vx and Vx+1 will then no longer overlay each other - Fig.8, [0037]) ([0007]; [0037]);

(15) A computer program product comprising a computer readable medium having computer readable program code embodied therein, executable by a computer for correcting a ground rule volition for a target via pair in a design, the program product comprising ([0039]):

program code for identifying a target via pair the violates a ground rule (The invention can also be used to eliminate certain undesirable structures such as stacked vias or can be used to fix other problems such as insufficient via-to -via spacing – Abstract; The invention first locates stacked vias by determining which vias are positioned above or below vias in adjacent wiring levels of the integrated circuit design (using a shapes-processing program) – [0007]; the invention first uses a shapes-processing program to find vias of interest … sets of vias that should be further spaced apart – [0025]); (Abstract; [0007]; [0025]); then

program code for generating a redundant via for a target via (the invention forms redundant via 20 to the left of via 10. This creates space for redundant via 21 which is a redundant via of via 12 – Fig.2, [0029]; the invention adds a redundant via … this

process is similar to the process of adding redundant vias discussed above – Fig.8, [0037]) of the target via pair (The invention first locates stacked vias by determining which vias are positioned above or below vias in adjacent wiring levels of the integrated circuit design – [0007]; the invention first uses a shapes-processing program to find vias of interest … sets of vias that should be further spaced apart – [0025]) where the redundant via corrects the ground rule violation (The invention can also be used to eliminate certain undesirable structures such as stacked vias or can be used to fix other problems such as insufficient via-to -via spacing – Abstract; the invention adds a redundant via and then removes the original via. In this way, vias on level Vx and Vx+1 will then no longer overlay each other - Fig.8, [0037]) (col.1, ll.49-54; col.4, ll.40-44; col.4, ll.55-57; col.5, ll.57-67; col.6, ll.1-7); (Abstract; [0002]; [0007]; [0025]; [0028]; [0029]; [0037]; [0038]); and

program code for removing the target via corresponding to the redundant via to correct the ground rule violation (the invention adds a redundant via and then removes the original via. In this way, vias on level Vx and Vx+1 will then no longer overlay each other - Fig.8, [0037]) ([0007]; [0037]);

5. As to claims 2-7, 9-14 and 16-20 Allen recites:

(2), (9), (16) The method/system/program, wherein the removing step includes removing the redundant vias ([0007]; [0026]);

(3), (4), (10), (11), (17), (18) The method/system/program, further comprising the step of distinguishing target via pairs from other structure (Abstract; [0007]; [0025]);

(5), (12), (19) The method/system/program, wherein the ground rule is a different-net spacing ground rule (Abstract; [0007]; [0025]);

(6), (13), (20) The method/system/program, wherein the generating step includes generating the redundant structure where no spacing ground rule violation occurs for a new technology (Abstract; [0004]; [0025]; [0041]);

(7), (14) The method/system, further comprising the steps of repeating the generating and removing steps for each level of a design ([0004]; [0007]; [0030]; [0032]; [0038]; [0041]).

REMARKS

6. Mostly Applicant argues: "Allen never discloses … correction of a ground rule violation".

Allen, for example, recites: "The invention can also be used to eliminate certain undesirable structures such as stacked vias or can be used to fix other problems such as insufficient via-to -via spacing - Abstract". Fixing insufficient via-to-via spacing or eliminating of undesirable structures such as stacked vias, both correspond to correction the ground rule violation of claims.

7. Next Applicant argues: "Allen never discloses … identification of a target via pair that violates a ground rule".

Allen, e.g., describes: "The invention first locates stacked vias by determining which vias are positioned above or below vias in adjacent wiring levels of the integrated circuit design (using a shapes-processing program) – [0007]". Allen also, e.g., teaches: "the invention first uses a shapes-processing program to find vias of interest … sets of

vias that should be further spaced apart – [0025]". Both examples correspond to identification of a target via par that violates a ground rule.

8. Examiner finds Applicant's arguments as none persuasive, because as indicated above the reference reads on the claims as presently written. For these reasons the prior rejections are maintained. However, Applicants' arguments are to look are well taken.

9. Accordingly, **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

N L

VUTHE SIEK
PRIMARY EXAMINER